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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,488	01/27/2004	Jayesh R. Bhakta	NETL.001DV3	9538

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EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,488	BHAKTA ET AL.	
	Examiner	Art Unit	
	Ly D Pham	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,11,13-17 and 21* is/are rejected.

7)☒ Claim(s) *2,8-10,12 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *040104 & 052804*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's Pre-Amendment filed March 02, 2004 has been entered.

2. Applicant's Information Disclosure Statements, IDSs, filed April 01 and May 28, 2004 have been considered by the examiner.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3 – 7, 11, 13 – 17, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawamura et al. (US Pat Pub 2003/0075789 A1) in view of Pettey et al. (US Pat 6,594,712 B1).

Regarding claims 1, 11, and 21, Kawamura et al. disclose a memory module comprising:

a printed circuit board (fig. 6, memory module with ICs mounted on a PCB);

a plurality of identical integrated circuits mounted in a first row and a second row onto at least one surface of the printed circuit board (fig. 6, two rows of identical memory ICs shown mounted on one side of the PCB);

a first register and a second register connected to the control logic bus for accessing data bits (fig. 6, the two identical ICs below the two rows of memory ICs and along the signal trace connector area).

Although Kawamura et al. did not clearly show the first register accessing a first range and a second range of data bits, and the second register accessing a third range and a fourth range of data bits, the first range and the second range of data bits being the first and second non-contiguous subsets of data word, and the third range and the fourth range of data bits being third and fourth non-contiguous subsets of data word, the feature has been disclosed by Pettey et al. (abstract: 'A plurality of programmable address range registers facilitates multiple of the direct transfers concurrently by dividing the dedicated address range into multiple sub-ranges'). Clearly, as the registers are capable of facilitating address ranges that are programmable by dividing the address range into multiple subranges, which are considered as subsets of the word, the subsets of data bits accessed by the registers are only one variation of address ranges being divided as disclosed by Pettey et al. Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to incorporate the multiple address sub-ranges programmable to the registers shown by Kawamura et al., to enable random mapping subsets of word bits to the plurality of internal buffers according predetermined address range of the local bus address space (abstract and col. 25, lines 50 – 52).

Regarding **claims 3 – 7, and 13 – 17**, Kawamura et al. also show the memory module of claim 1, wherein the PCB has a line of bilateral symmetry which bisects the PCB into a first lateral half and a second lateral half (fig. 6, line of bilateral symmetry would be the imaginary line perpendicular and crosses the midpoint of the longitudinal edge of the PCB). As a result, the first row and the second row are substantially perpendicular and symmetric to the line of bilateral symmetry.

Allowable Subject Matter

5. **Claims 2, 8 – 10, 12, and 18 – 20** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

The prior arts teach memory module of claim 1, except:

wherein the first range of data bits comprise data bits 0 to 15; the second range of data bits comprise data bits 32 – 47; the third range of data bits comprise data bits 16 – 31; and the fourth range of data bits comprise data bits 48 - 63.

And

wherein the first register addresses the identical ICs located in the first row and in the second row on a first lateral portion of the PCB, the second register addresses the identical ICs located in the first row and in the second row on a second lateral portion of the PCB.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. When responding to the office action, Applicant(s) are advised to provide the examiner with the page and line numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

10. Any inquiry concerning this communication on earlier communications from the examiner should be directed to Ly Pham, whose telephone number is **571-272-1793**. The examiner can normally be reached on Monday – Friday from 8:30am to 5:00pm, alternate Friday off. The examiner's supervisor, David Nelms, can be reached at **571-272-1787**. The fax number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Ly Pham

August 17, 2004